Week 8

The 8088 and 8086 Microprocessors
8086 and 8088 Microprocessors

- 8086 announced in 1978; 8086 is a 16 bit microprocessor with a **16 bit data bus**
- 8088 announced in 1979; 8088 is a 16 bit microprocessor with an **8 bit data bus**
- Both manufactured using High-performance Metal Oxide Semiconductor (HMOS) technology
- Both contain about 29000 transistors
- Both are packaged in 40 pin dual-in-line package (DIP)
- Address lines A0-A7 and Data lines D0-D7 are multiplexed in 8088. These lines are labelled as AD0-AD7.
  - By multiplexed we mean that the same physical pin carries an address bit at one time and the data bit another time
- Address lines A0-A15 and Data lines D0-D15 are multiplexed in 8086. These lines are labelled as AD0-AD15.
8088 and 8086 Microprocessors

LOST IN MAXIMUM MODE
Minimum-mode and Maximum-mode Systems

- 8088 and 8086 microprocessors can be configured to work in either of the two modes: the minimum mode and the maximum mode

✔ Minimum mode:
  - Pull MN/MX to logic 1
  - Typically smaller systems and contains a single microprocessor
  - Cheaper since all control signals for memory and I/O are generated by the microprocessor.

✔ Maximum mode
  - Pull MN/MX logic 0
  - Larger systems with more than one processor (designed to be used when a coprocessor (8087) exists in the system)
**PINs on microprocessor**

Signals common to both minimum and maximum systems

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A7-AD0</td>
<td>Address/data bus</td>
<td>Bidirectional, 3-state</td>
</tr>
<tr>
<td>A15-A8</td>
<td>Address bus</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>A19/S6-A16/S3</td>
<td>Address/status</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>MN/MX</td>
<td>Minimum/maximum Mode control</td>
<td>Input</td>
</tr>
<tr>
<td>RD</td>
<td>Read control</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>TEST</td>
<td>Wait on test control</td>
<td>Input</td>
</tr>
<tr>
<td>READY</td>
<td>Wait state control</td>
<td>Input</td>
</tr>
<tr>
<td>RESET</td>
<td>System reset</td>
<td>Input</td>
</tr>
<tr>
<td>NMI</td>
<td>Nonmaskable Interrupt request</td>
<td>Input</td>
</tr>
<tr>
<td>INTR</td>
<td>Interrupt request</td>
<td>Input</td>
</tr>
<tr>
<td>CLK</td>
<td>System clock</td>
<td>Input</td>
</tr>
<tr>
<td>Vcc</td>
<td>+5 V</td>
<td>Input</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>Input</td>
</tr>
</tbody>
</table>
## PINs on microprocessor

### Minimum mode unique signals

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>HOLD</td>
<td>Hold request</td>
<td>Input</td>
</tr>
<tr>
<td>HLDA</td>
<td>Hold acknowledge</td>
<td>Output</td>
</tr>
<tr>
<td>WR</td>
<td>Write control</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>IO/M</td>
<td>IO/memory control</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>DT/R</td>
<td>Data transmit/receive</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>DEN</td>
<td>Data enable</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>SSO</td>
<td>Status line</td>
<td>Output, 3-state</td>
</tr>
<tr>
<td>ALE</td>
<td>Address latch enable</td>
<td>Output</td>
</tr>
<tr>
<td>INTA</td>
<td>Interrupt acknowledge</td>
<td>Output</td>
</tr>
</tbody>
</table>
8088 Minimum-mode block diagram

Power supply

- $V_{CC}$
- GND

Address/data bus

- $A_{D0}-A_{D7}$
- $A_{16}/S_3$-$A_{19}/S_6$
- $A_{8}-A_{15}$
- ALE
- SSO
- IO/M
- DT/R
- RD
- WR
- DEN
- READY

Interrupt interface

- INTR
- INTA
- TEST
- NMI
- RESET

DMA interface

- HOLD
- HLDA

Mode select

- MN/MX

Clock

- CLK
Due to chip packaging limitations in the 1970s, there was great effort to use the minimum number of pins for external connections.

- Intel multiplexed address & data buses, using the same pins to carry two sets of information: address & data.

- Pins 9-16 (AD0–AD7) are used for both data and addresses in 8088.
  - AD stands for "address/data."

- The ALE (address latch enable) pin signals whether the information on pins AD0–AD7 is address or data.

Fig. 9-1a 8088 in minimum mode
9.1: 8088 MICROPROCESSOR data bus

- When 8088 sends out an address, it activates (sets high) the **ALE**, to indicate the information on pins AD0–AD7 is the *address* (A0–A7).
  - This information must be *latched*, then pins AD0–AD7 are used to carry data.

- When data is to be sent out or in, **ALE** is low, which indicates that AD0–AD7 will be used as *data* buses (D0–D7).

- The process of separating address and data from pins AD0–AD7 is called *demultiplexing*.
9.1: 8088 MICROPROCESSOR address bus

- 8088 has 20 address pins (A0–A19), allowing it to address a maximum of one megabyte of memory ($2^{20} = 1M$).
  - To demultiplex address signals, a latch must be used to grab the addresses.

- Widely used is the 74LS373 IC, also 74LS573, a 74LS373 variation.
  - AD0 to AD7 go to the 74LS373 latch, providing the 8-bit address A0–A7.
  - A8–A15 come directly from the microprocessor (pins 2–8 & pin 39).
- The last 4 bits of the address come from A16–A19, pin numbers 35–38.

Fig. 9-1a 8088 in minimum mode
9.1: 8088 MICROPROCESSOR address bus

The most widely used latch is the 74LS373 IC. Also used is the 74LS573, a 74LS373 variation.

Fig. 9-2 Role of ALE in address/data demultiplexing

Fig. 9-3 74 LS373 D Latch
In any system, all addresses must be latched to provide a stable, high-drive-capability address bus.
9.1: 8088 MICROPROCESSOR control bus

- 8088 can access both memory and I/O devices for read and write operations, four operations, which need four control signals:
  - MEMR (memory read); MEMW (memory write).
  - IOR (I/O read); IOW (I/O write).
9.1: 8088 MICROPROCESSOR control bus

- 8088 provides three pins for control signals:
  - RD, WR, and IO/M.
    - RD & WR pins are both active-low.
    - IO/M is low for memory, high for I/O devices.

![Control signal generation diagram](image)
9.1: 8088 MICROPROCESSOR control bus

- 8088 provides three pins for control signals:
  - RD, WR, and IO/M.
    - RD & WR pins are both active-low.
    - IO/M is low for memory, high for I/O devices.

Four control signals are generated:
- IOR; IOW;
- MEMR; MEMW.

All of these signals must be active-low.

<table>
<thead>
<tr>
<th>RD</th>
<th>WR</th>
<th>IO/M</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>MEMR</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>MEMW</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>IOR</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>IOW</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>x</td>
<td>Never happens</td>
</tr>
</tbody>
</table>
9.1: 8088 MICROPROCESSOR control bus

Use of simple logic gates (inverters and ORs) to generate control signals. CPLD (complex programmable logic devices) are used in today’s PC chipsets.

Fig. 9-5 Address, Data, and Control Buses in 8088-based System
Minimum Mode Interface

- Address/Data bus: 20 bits/8 bits (AD0-AD7) multiplexed for 8088
- Address/Data bus: 20 bits/16 bits (AD0-AD15) multiplexed for 8086
- Status signals: A_{16} - A_{19} multiplexed with status signals S_3 - S_6 respectively
  - **S3 and S4 together** form a 2 bit binary code that identifies which of the internal segment registers were used to generate the physical address that was output on the address bus during the current bus cycle.
  - **S5** is the logic level of the IF,
  - **S6 is always logic 0.** S0,S1,S2 used in maxmode (later)

<table>
<thead>
<tr>
<th>S4</th>
<th>S3</th>
<th>Address status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Alternate (relative to ES segment)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Stack (relative to SS Segment)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Code/None (relative to CS segment or a default zero)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Data (relative to DS segment)</td>
</tr>
</tbody>
</table>
Minimum Mode Interface

• Control Signals: (8088)
  ✓ **Address Latch Enable (ALE)** is a pulse to logic 1 that signals external circuitry when a valid address is on the bus. This address can be latched in external circuitry on the 1-to-0 edge of the pulse at ALE.
  ✓ **IO/M line**: memory or I/O transfer is selected (complement for 8086)
  ✓ **DT/R line**: direction of data is selected
  ✓ **RD line**: =0 when a read cycle is in progress
  ✓ **WR line**: =0 when a write cycle is in progress
  ✓ **DEN line**: (Data enable) Enables the external devices to supply data to the processor. Used when sharing memory with another processor.
9.1: 8088 MICROPROCESSOR address bus

The most widely used latch is the 74LS373 IC. Also used is the 74LS573, a 74LS373 variation.

**Fig. 9-2** Role of ALE in address/data demultiplexing

**Fig. 9-3** 74 LS373 D Latch

**Function Table**

<table>
<thead>
<tr>
<th>Control</th>
<th>Enable</th>
<th>D</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>Q0</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Z</td>
</tr>
</tbody>
</table>
Control Signals: (8088)

SSO (System Status Output) line (only for 8088)
=1 when data is read from memory and =0 when code is read from memory

<table>
<thead>
<tr>
<th>IO/M</th>
<th>DT/R</th>
<th>SS0</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Interrupt Acknowledge</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Memory Read</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Memory Write</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Halt</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Opcode Fetch</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>I/O Read</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>I/O Write</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Passive</td>
</tr>
</tbody>
</table>
Minimum Mode Interface

✓ **BHE (Bank High Enable) line** (8086 only) :=0 for most significant byte of data and also carries $S_7=1$

<table>
<thead>
<tr>
<th>BHE#</th>
<th>A0</th>
<th>Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Whole word (16-bits)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>High byte to/from odd address</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Low byte to/from even address</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>No selection</td>
</tr>
</tbody>
</table>

This is how memory is accessed using these signals:
Data Transfer

Figure 8-16  (a) Byte transfer by the 8088. (b) Word transfer by the 8088.
A bus cycle (machine cycle) defines the basic operation that a microprocessor performs to communicate with external devices.

Examples of bus cycles are memory read, memory write, input/output read and input/output write.

A bus cycle corresponds to a sequence of events that starts with an address being output on the system bus followed by a read or write data transfer.

During these operations, a series of control signals are also produced by the MPU to control the direction and timing of the bus.

Each bus cycle consists of at least four clock periods: T1, T2, T3, and T4.

These clock periods are also called the T-States.
Bus Cycle and Time States

Bus Cycles

CLK
ALE
M/IO
ADDR/STATUS
ADDR/DATA
RD
READY
DTR
DEN
WR
9.1: 8088 MICROPROCESSOR
bus timing of the 8088

- 8088 uses 4 clocks for memory & I/O bus activities.
  - In read timing, **ALE** latches the address in the first clock cycle.
  - In the second and third cycles, the read signal is provided.
  - By the end of the fourth, data must be at the CPU pins.
  - The entire read or write cycle time is only 4 clock cycles.

If reading/writing takes more than 4 clocks, wait states (WS) can be requested from the CPU.

![Fig. 9-6 ALE Timing](image-url)
Bus Cycle and Time States

T1 - start of bus cycle. Actions include setting control signals (or S0-S2 status lines) to give the required values for ALE, DTR IO/M putting a valid address onto the address bus.

T2 - the RD or WR control signals are issued, DEN is asserted and in the case of a write, data is put onto the data bus. The DEN turns on the data bus buffers to connect the CPU to the external data bus. The READY input to the CPU is sampled at the end of T2 and if READY is low, a wait state $T_w$ (one or more) is inserted before T3 begins.

T3 - this clock period is provided to allow memory to access the data. If the bus cycle is a read cycle, the data bus is sampled at the end of T3.

T4 - all bus signals are deactivated in preparation for the next clock cycle. The 8088 also finishes sampling the data (in a read cycle) in this period. For the write cycle, the trailing edge of the WR signal transfers data to the memory or I/O, which activates and write when WR returns to logic 1 level.
Read Cycle of the 8086

Bus Timing for a Read Operation
Read Cycle

• Each BUS CYCLE (machine cycle) on the 8086 equals four system clocking periods (T states).
• The clock rate is 5MHz, therefore one Bus Cycle is 800ns.
• Memory specs (memory access time) must match constraints of system timing.
• For example, bus timing for a read operation shows almost 600ns are needed to read data.
• However, memory must access faster due to setup times, e.g.
• Address setup and data setup.
• This subtracts off about 150ns.
• Therefore, memory must access in at least 450ns minus another 30-40ns guard band for buffers and decoders.
• 420ns DRAM required for the 8086.
Write Cycle in 8088/8086 Minmode

One Bus Cycle

T₁  T₂  T₃  T₄

CLK

Address

Valid Address

Address/Data

Address  Data written to memory

WR

Simplified 8086 Write Bus Cycle
9.1: 8088 MICROPROCESSOR other pins

- Pins 24–32 have different functions depending on whether 8088 is in minimum or maximum mode.
  - In maximum mode, 8088 needs supporting chips to generate the control signals.

Fig. 9-1a 8088 in minimum mode
### 9.1: 8088 MICROPROCESSOR other pins

Functions of 8088 pins 24–32 in minimum mode.

#### Table 9-2: Pins 24–32 in Minimum Mode

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name and Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>INTA (interrupt acknowledge) Active-low output signal. Informs interrupt controller that an INTR has occurred and that the vector number is available on the lower 8 lines of the data bus.</td>
</tr>
<tr>
<td>25</td>
<td>ALE (address latch enable) Active-high output signal. Indicates that a valid address is available on the external address bus.</td>
</tr>
<tr>
<td>26</td>
<td>DEN (data enable) Active-low output signal. Enables the 74LS245. This allows isolation of the CPU from the system bus.</td>
</tr>
<tr>
<td>27</td>
<td>DT/R (data transmit/receive) Active-low output signal used to control the direction of data flow through the 74LS245 transceiver.</td>
</tr>
<tr>
<td>28</td>
<td>IO/M (input-output or memory) Indicates whether the address bus is accessing memory or an I/O device. In the 8088, it is low when accessing memory and high when accessing I/O. This pin is used along with RD and WR pins to generate the four control signals MEMR, MEMW, IOR, and IOW.</td>
</tr>
</tbody>
</table>
9.1: 8088 MICROPROCESSOR other pins

Functions of 8088 pins 24–32 in minimum mode.

Table 9-2: Pins 24–32 in Minimum Mode

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name and Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>29</td>
<td>WR (write) Active-low output signal. Indicates that the data on the data bus is being written to memory or an I/O device. Used along with signal IO/M (pin 28) to generate the MEMW and IOW control signals for write operations.</td>
</tr>
<tr>
<td>30</td>
<td>HLDA (hold acknowledge) Active-high output signal. After input on HOLD, the CPU responds with HLDA to signal that the DMA controller can use the buses.</td>
</tr>
<tr>
<td>31</td>
<td>HOLD (hold) Active-high input from the DMA controller that indicates that the device is requesting access to memory and I/O space and that the CPU should release control of the local buses.</td>
</tr>
<tr>
<td>32</td>
<td>RD (Read) Active-low output signal. Indicates that the data is being read (brought in) from memory or I/O to the CPU. Used along with signal IO/M (pin 28) to generate MEMR and IOR control signals for read operations.</td>
</tr>
</tbody>
</table>
Minimum Mode Interface

- DMA (Direct Memory Access) Interface Signals:
  - **HOLD**: External device puts logic level 1 to HOLD input to take control of the bus for DMA request. (sampled at every rising edge of the CLK)
  - **HLDA** (Hold acknowledge): Processor responds by putting logic level 1 to HLDA. (at the end of T4)
  - In this state; Address and Data lines, SSO, IO/M, DT/R, RD, WR, DEN signals are all put to high-Z state

![HOLD timing diagram](image)
9.1: **8088 MICROPROCESSOR other pins**

- **MN/MX** (minimum/maximum) - minimum mode is selected by connecting MN/MX (pin number 33) directly to +5 V.
  - Maximum mode is selected by grounding this pin.
- **CLOCK** - an input signal, connected to the 8284 clock generator.
Minimum Mode Interface

- **Interrupt signals:**
  - **INTR (Interrupt request)** := 1 shows there is a service request, sampled at the final clock cycle of each instruction acquisition cycle.
  - **INTA** @T1 tri-states the Address Bus. Processor responds with two pulses going to 0 when it services the interrupt and waits for the interrupt service number after the second pulse.
9.1: 8088 MICROPROCESSOR other pins

- **TEST** - in maximum mode, an input from the 8087 math coprocessor to coordinate communications. Processor suspends operation when=1. Resumes operation when=0. Used to synchronize the processor to external events. (All 8087-capable compilers and assemblers automatically generate a `WAIT` instruction before each coprocessor instruction. The `WAIT` instruction tests the CPU's `TEST` pin and suspends execution until its input becomes "LOW". When `TEST=0`, `WAIT` instruction is like `NOP`.
  - In all 8086/8087 systems, the 8086 /TEST pin is connected to the 8087 BUSY pin. As long as the EU executes a coprocessor instruction, it forces its BUSY pin "HIGH"; thus, the WAIT opcode preceding the coprocessor instruction stops the CPU until any still-executing coprocessor instruction has finished)
  - Not used in minimum mode!.
9.1: 8088 MICROPROCESSOR other pins

- **RESET** - terminates present activities of the processor when a *high* is applied to the **RESET** input pin.
- **RESET** : $=0$. Need at least 4 clock cycles. Issuing reset causes the processor to fetch the first instruction from the memory FFFF:0000h.

A presence of *high* will force the microprocessor to stop all activity and set the major registers to the values shown at right.

<table>
<thead>
<tr>
<th>Register</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS</td>
<td>FFFF</td>
</tr>
<tr>
<td>IP</td>
<td>0000</td>
</tr>
<tr>
<td>DS</td>
<td>0000</td>
</tr>
<tr>
<td>SS</td>
<td>0000</td>
</tr>
<tr>
<td>ES</td>
<td>0000</td>
</tr>
</tbody>
</table>

Table 9-3: IP and Segment Register Contents after Reset
Interrupt Signals cont’d

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Logic</th>
<th>Disabled by SW?</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMI</td>
<td>Rising Edge</td>
<td>No</td>
<td>High</td>
</tr>
<tr>
<td>INTR</td>
<td>High</td>
<td>Yes</td>
<td>Low</td>
</tr>
</tbody>
</table>

**NMI (Nonmaskable interrupt)**: A leading edge transition causes the processor to go to the interrupt routine after the current instruction is executed.

**NMI** (nonmaskable interrupt) - an edge-triggered (low to high) input signal to the processor that will make the microprocessor jump to the interrupt vector table after it finishes the current instruction.

- Cannot be masked by software.
Minimum Mode Interface

- **READY** Control line:
  - can be used to insert wait states into the bus cycle so that it is extended by a number of clock periods.
  
**READY** - an input signal, used to insert a wait state for slower memories and I/O. It inserts wait states when it is **low**.

- If the access time for a memory device is longer than the memory access time calculated, need to give extra clock periods, **wait state Tw**, for memory.

- The **READY** input is sampled at the end of **T2** and again, if applicable, in the middle of **Tw**. If **READY** is a logic 0 on 1-to-0 clock transition, then Tw is inserted between T2 and T3. And will check for logic 1 on 0-to-1 clock transition in the middle of Tw to see if it shall go back T3.

- During the wait state, signals on the buses remain the same as they were at the start of the WAIT state.

- By having the **WAIT** state, slow memory and devices has at least one more cycle (200ns for 5 MHz 8088) to get its data output.

(a) 8088/86 READY Input Timing
Read Cycle of the 8086 - minimum mode

- BHE is output along with the address during T1
- Data can be read during T3 over all 16 data bus lines
- M/IO replaces IO/M
- SSO status signal is not produced
Address Bus Latches and Buffers

![Diagram of Address Bus Latches and Buffers](image)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC</td>
<td>Enable C</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
</tr>
</tbody>
</table>
Address Latch Circuit

- ALE
- BHE

Diagram showing the connection of 74F373 latches and address lines AD0-AD15, A16-A19, and A16L-A19L, BHE.
Data Bus Transceiver Circuit

<table>
<thead>
<tr>
<th>GBAR ENABLE</th>
<th>DIR</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>B data to A</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>A data to B</td>
</tr>
<tr>
<td>H</td>
<td>x</td>
<td>Isolation</td>
</tr>
</tbody>
</table>
Buffered Systems

- Buffering (boosting) of the control, data, and address busses to provide sufficiently strong signals to drive various IC chips
  - When a pulse leaves an IC chip it can lose some of its strength depending on how far away the receiving IC is located
  - Plus the more pins a signal is connected to (i.e., fanout) the stronger the signal must be to drive them all which requires bus buffering
  - bus buffering = boosting the signals travelling on the busses
  - unidirectional bus 74LS244
  - bidirectional bus 74LS245
FIGURE 9-5 The 8088 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8088-based systems.
Fully buffered 8088
8086 System
Fully Buffered 8086
Memory Interface

- 8088 provides three pins for control signals:
  - RD, WR, and IO/M.
- RD & WR pins are both active-low.
- IO/M is low for memory, high for I/O devices.